Single Event Upset Test Results on a Prescalar Fabricated in IBM's 5HP Silicon Germanium Heterojunction Bipolar Transistors BiCMOS Technology

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***Abstract*--This paper presents heavy ion and proton SEE test results on an IBM designed high speed prescaler fabricated in germanium doped Silicon (SiGe) heterojunction bipolar transistors (HBT). These are the first published results on this technology.**

I. INTRODUCTION

IBM currently has three distinct SiGe Heterojunction Bipolar Transistor (HBT) BiCMOS technologies either under development or fully developed. The 5HP series, available through MOSIS, is their baseline SiGe BiCMOS technology. The 6HP series features laterally scaled HBT and fully scaled CMOS. The 7HP series includes both laterally and vertically scaled HBT and fully scaled CMOS. The data presented in this paper are for a device fabricated in the 5HP HBT technology.

Cressler et al. [1 and references therein] have demonstrated that IBM's SiGe 5HP HBT technology is radiation tolerant to nearly a Megarad(Si), while the CMOS was tolerant to nearly 75 krad(Si).

Marshall et al. [2] evaluated heavy ion and pulsed laser Single Event Upset (SEU) susceptibility of a circuit hardening attempt in 5HP series HBT for a potential SEU critical application. This study showed this technology to be very sensitive to SEU. Their work identified the critical need to improve and fully characterize the SEU response of the SiGe technology.

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In this paper we present the first published SEU data on a fully functional device fabricated in an unhardened SiGe HBT technology.

II. DEVICE TECHNOLOGY

Fig. 1 shows a schematic of the device cross-section of the SiGe HBT. The SiGe HBT has a planar, self-aligned structure with a conventional poly emitter contact, silicided extrinsic base, and deep- and shallow-trench isolation. Details of the fabrication process can be found in [3]. The n-p-n layers of the intrinsic transistor and the p-type substrate form a n-p-n-p multi-layer structure. The substrate is usually biased at the lowest potential in order to reverse bias the collector-substrate junction.

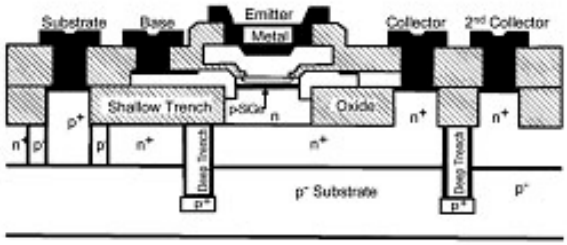

Fig. 1. The schematic cross section of the SiGe HBT.

Key performance metrics of the 5HP SiGe HBT's include:

- 47 GHz (for the device used in this study) cut-off frequency (fT);
- 60 GHz (for the device used in this study) maximum oscillation frequency (fmax);
- Better than 0.5dB minimum noise figure (NFmin) at 2 GHz;
- Excellent power added efficiency of 65% at 900 MHz;
- Excellent linearity efficiency of 10 at 2 GHz;
- Emitter width of 0.5 mm;
- NMOS and PMOS transistors with a drawn gate length of 0.5 mm;
- Substrate resistivity of 10 to 20 Ω-cm.

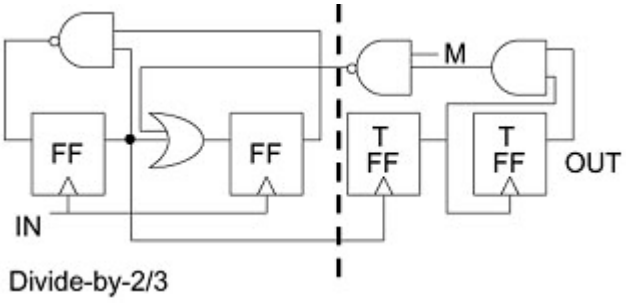

Fig. 2. Block diagram of IBM prescaler.

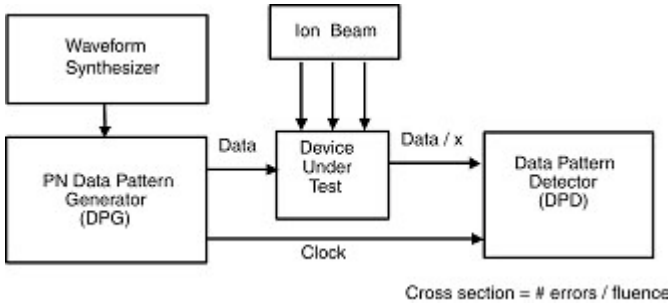

Fig. 3. Block diagram of the test setup.

III. Device Under Test

The Device Under Test (DUT) is a dual-modulus divide-by-8 or by-9 prescaler circuit [4]. This circuit, which is typically used as a core component of a frequency synthesizer, provides an output signal having a frequency equal to 1/8 or 1/9 of the input-signal frequency. A static control signal sets the prescaler to either the divide-by-8 or divide-by-9 mode. The circuit is implemented in IBM's 5HP SiGe BiCMOS technology and occupies an area of 0.3 mm^2. It contains 193 HBT's (used for the high-frequency section) and 6 MOS transistors (used to buffer the static modulus control signal).

A block diagram of the prescaler is shown in Fig. 2. The input signal is received by a buffer (not shown) which drives the clock inputs of two flip-flops (FF's). When the modulus control input M equals logic 0 these two FF's divide the input by 2. If the modulus is set to logic 1 then these two FF's divide the input by 2 for most of the time, however, every 9^{th} clock cycle, these FF's function as a divide-by-3. The two remaining toggle flip-flops (TFF's) then divide the output of the first FF by 4, to achieve the 8 (if M=0) or 9 (if M=1) overall division ratio. An output buffer (not shown) drives the signal off-chip.

IV. Test Setup

The testing was done using the BA3600 Bit Error Rate Tester (BERT) from SyntheSys Research, Inc (See Fig. 3). It generates the input pattern to the DUT and detects errors on the DUT output. The Data Pattern Generator (DPG) and Data Pattern Detector (DPD) are independent on the BA3600. A Hewlett Packard waveform synthesizer from (HP83712B) provides the input clock frequency to the BA3600.

The DPG generated a square-wave data signature with 50% duty cycle at the frequency of the waveform synthesizer. This data is passed to the prescaler which divides the input by 8 (if M=0) or 9 (if M=1). The output of the prescaler is passed it to the DPD for error detection and error signature storage. The expected data pattern from the prescaler is captured prior to irradiation and stored in DPD so that it can be used to detect errors in the prescaler output during an irradiation. The DPG also provides the clock input to the DPD.

Synchronization with the output data pattern of the prescaler has to be optimized prior to irradiation. This was done by delaying the clock from –640 ps to +640 ps.

Once the optimization was reached, the DUT was placed in the particle beam and the DPD continuously compared the data pattern from the DUT against the expected pattern. For all mismatches, the error signature was recorded along with its location in the data stream. Consecutive mismatches of 100 or more are considered as a synchronization error. When this occurred an automatic re-synchronization (resync) was initiated and achieved by the DPD. All data that were determined to be an error, either a resync or bit errors, were stored in real-time by the BA3600.

The data storage capability allowed the data to be reduced so that two types of error signatures could be tallied during each exposure: 1) number of re-syncs 2) number of sequential bits in error (or equivalently, the duration of an error in clock cycles).

V. Single Event Upset Failure Modes

Bit errors induced by single particle events in the active flip flops will act as an extra clock signal, causing the data to lose synchronization with the clock. This is also true for the single particles events in the OR and NANDs used in either of the divide-by modes and in the AND in divide-by-9 mode. These events will be detected as a resynchronization of the BERT.

A critical path in the prescaler circuit is through the OR gate and second FF. This is active only when M=1. Thus, one failure mode exhibited by this circuit is if the output frequency equals 1/8 of the input frequency despite the M=1 (divide-by-9) modulus control being asserted, indicating that this critical path has failed. Another similar failure mode is if the output frequency is 1/9 of the input frequency, despite M=0 (divide-by-8 mode). These events will be detected as a BERT resynchronization.

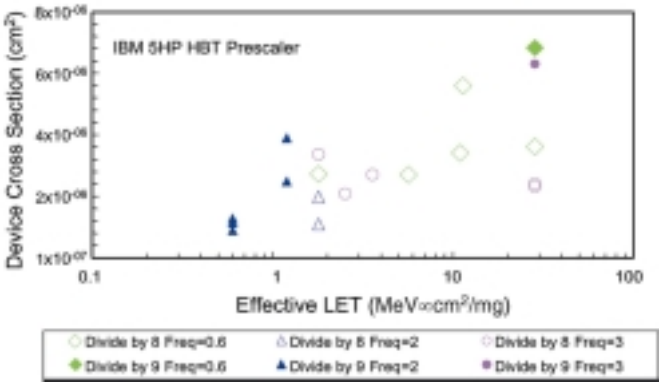

Fig. 4. Heavy ion induced resync results for both modes at various frequencies.

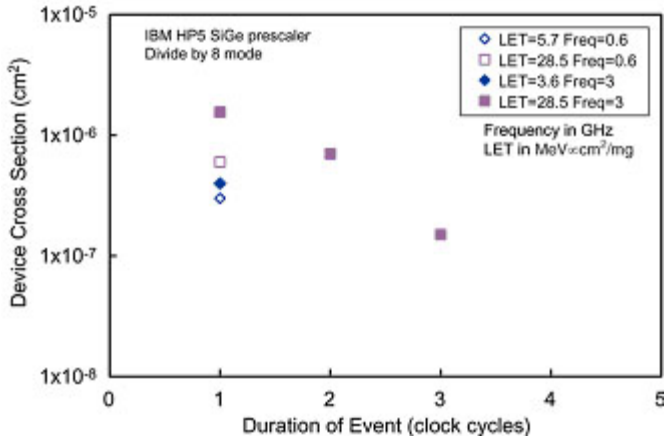

Fig. 5. Duration of bit errors for the divide-by-8 mode.

Particle induced errors in the output buffer will be detected as a sequence of bit errors. These will not cause a resynchronization of the BERT.

VI. TEST FACILITIES

Heavy ion tests were preformed at Texas A&M University Cyclotron Laboratory. The table below list the ions used along with their Linear Energy Transfer (LET). All other LET values were achieved by rotating the angle on incidence of the ion beam (i.e., effective LET).

Table I. Ion species and LETs used for this study.

Species	LET (MeV∞cm²/mg)
O-16	0.6
Ne-22	1.8
Ar-40	5.7
Kr-84	28.5

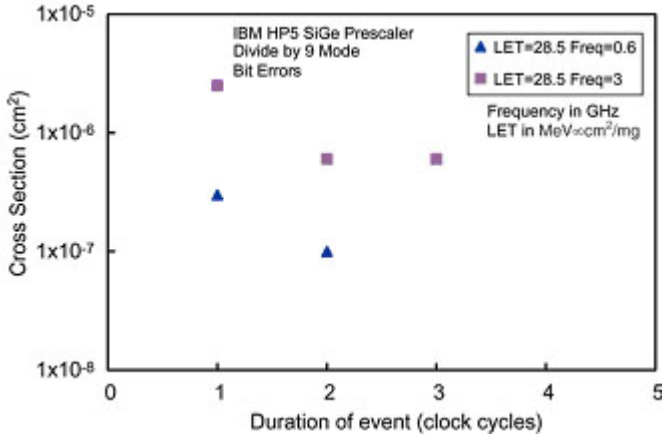

Fig. 6. Duration of bit errors not requiring a re-sync for the divide-by-9 mode.

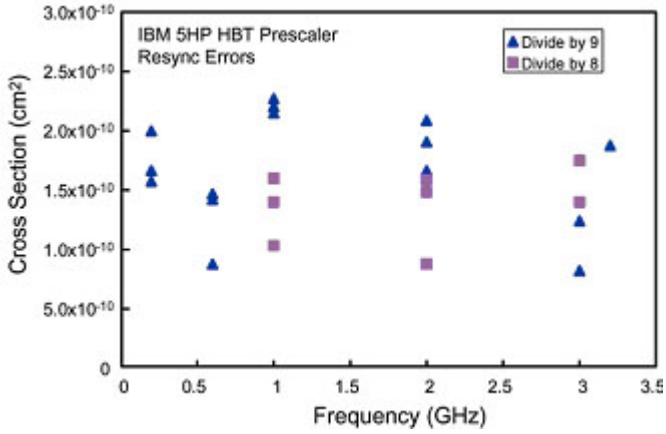

Fig. 7. Proton-induced resyncs results for both modes over several operating frequencies.

Proton test were carried out at University of California at Davis using a 63 MeV proton beam.

VII. TEST RESULTS

A. *Heavy Ion Test Result*

Fig. 4 shows the cross section data obtained for errors producing a resync during heavy ion testing. The data are plotted for various frequencies and for both modes of operation, i.e. divide-by-8 and divide-by-9. (Note that this is a linear-log plot.)

The first notable characteristic of this data is that both modes are very sensitive to low LET ions. Recall that there are only a few hundred transistors in this design. The data approaches its saturation value for LETs well below 10 MeV·cm^2/mg.

The second thing to notice in this data is that there is no correlation with frequency. The data near an LET of 1.8 MeV·cm^2/mg shows that the cross section for 0.6 GHz is between the 2 and 3 GHz data, data taken at 3 GHz begin slightly higher that at 0.6 GHz data. While at a 28.5

MeV·cm^2/mg the 0.6 GHz cross section data is greater than the 3 GHz data.

Next we look at the bit error data for heavy ion exposures (most likely due to events in the MOS output buffers). The data analysis showed that bit errors could last for more than one clock cycle [also observed in reference 2]. The data for the divide-by-8 mode are given in Fig. 5 and that for divide-by-9 mode are in Fig. 6. The plots give the cross section for a bit error with a given duration. All exposures were carried out to a fluence of 1x10^7 particles/cm^2.

B. Proton Test Results

Fig. 7 gives the 63 MeV proton test results for various frequencies for both modes of operation. These data clearly show the lack of correlation between frequency and cross section for errors requiring resyncs.

Bit errors were also observed during proton testing. The maximum bit error duration was two clock cycles. The cross section was about 3x10-^{12} cm^2.

VIII. ACKNOWLEDGMENTS

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